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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : 09/441,119 Applicant : Oliver L. Richards, et al. Filed : November 17, 1999 T.C./A.U. : 2611 Examiner : Usha Raman Docket No. : ALLEG-017PUS Customer No. : 022494		Confirmation No.: 3874

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26 April 2004
Date of Signature
and Mail Deposit

By: Judith C. Crowley
Judith C. Crowley
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Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

SUBSTITUTE DECLARATION UNDER 37 CFR §1.131

1. I, Paul M. Greenland, am a co-inventor of a U.S. Patent Application entitled "Low Noise Block Supply and Control Voltage Regulator" now pending before the U. S. Patent Office as Application No. 09/441,119.

2. Prior to December 1998, I, along with co-inventor Oliver L Richards, conceived of the invention described in U. S. Patent Application No. 09/441,119, as evidenced by a

schematic captioned "LNB BUCK/BOOST PROPOSAL" and attached hereto as Exhibit A.

3. Following conception, I worked on developing a product incorporating the technology described in U. S. Patent Application No. 09/441,119, as evidenced by a schematic captioned "LNB BUCK REGULATOR PROPOSAL," dated 31 March 1999, and attached hereto as Exhibit B as well as a Product Preview datasheet for the 8284 Product of Allegro Microsystems, Inc. dated 19 July 1999 and attached hereto as Exhibit C.

4. The subject patent application was filed in the U.S. Patent Office on November 17, 1999.

5. All of the statements made herein are of my own knowledge and are true, these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under § 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application and any patent issuing thereon, or any patent to which this verified statement is applied.

4/19/04
Date of Signature

By: Paul Greenland
Paul M. Greenland

Exhibit A to 1.131 Declaration
U.S. Patent Application No.
09/441,119

24V
~~12V~~

LNB ~~Boost~~ Proposal
Buck

13.7, 15.7, 19.7 20.7 Volts

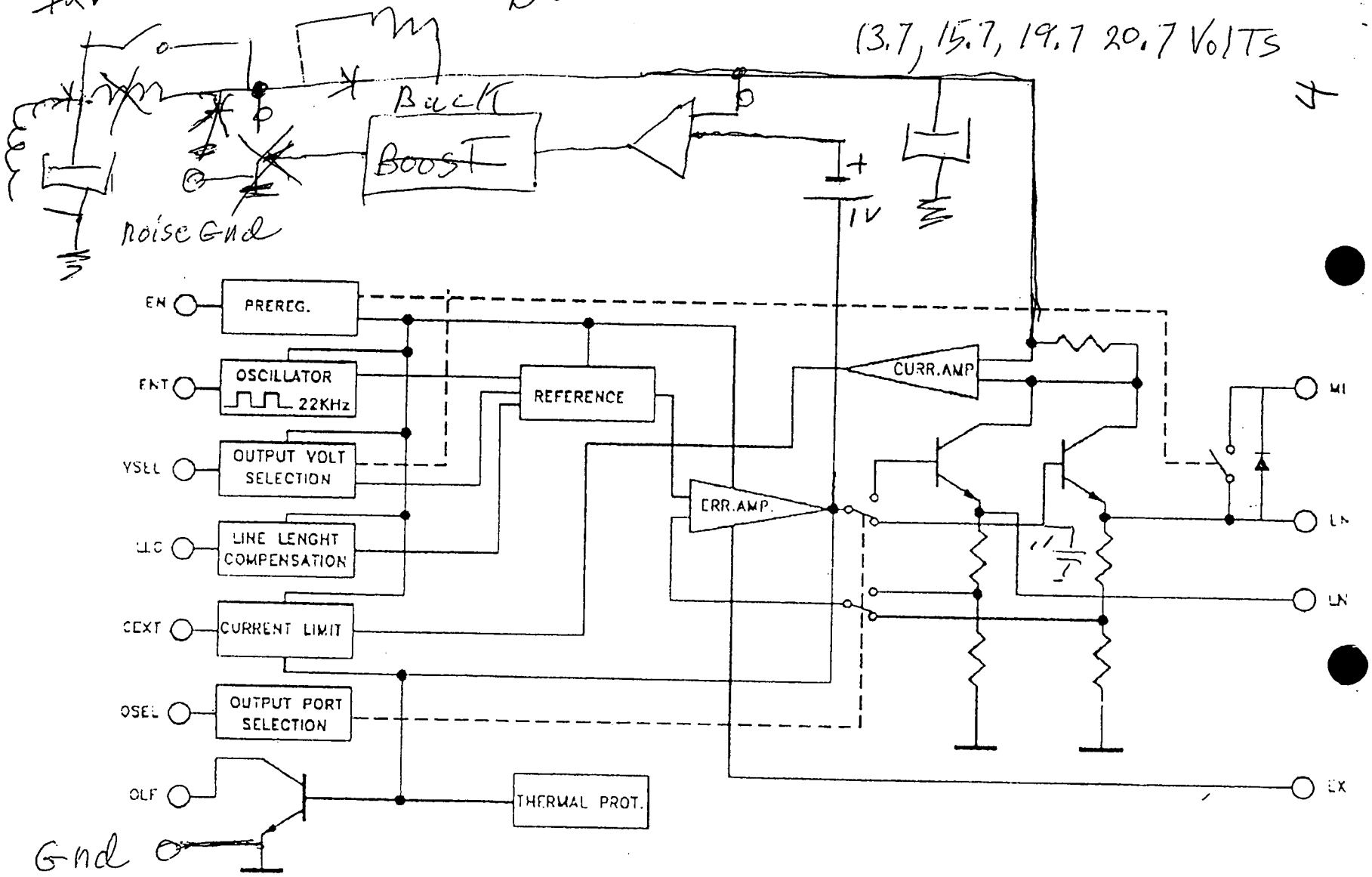
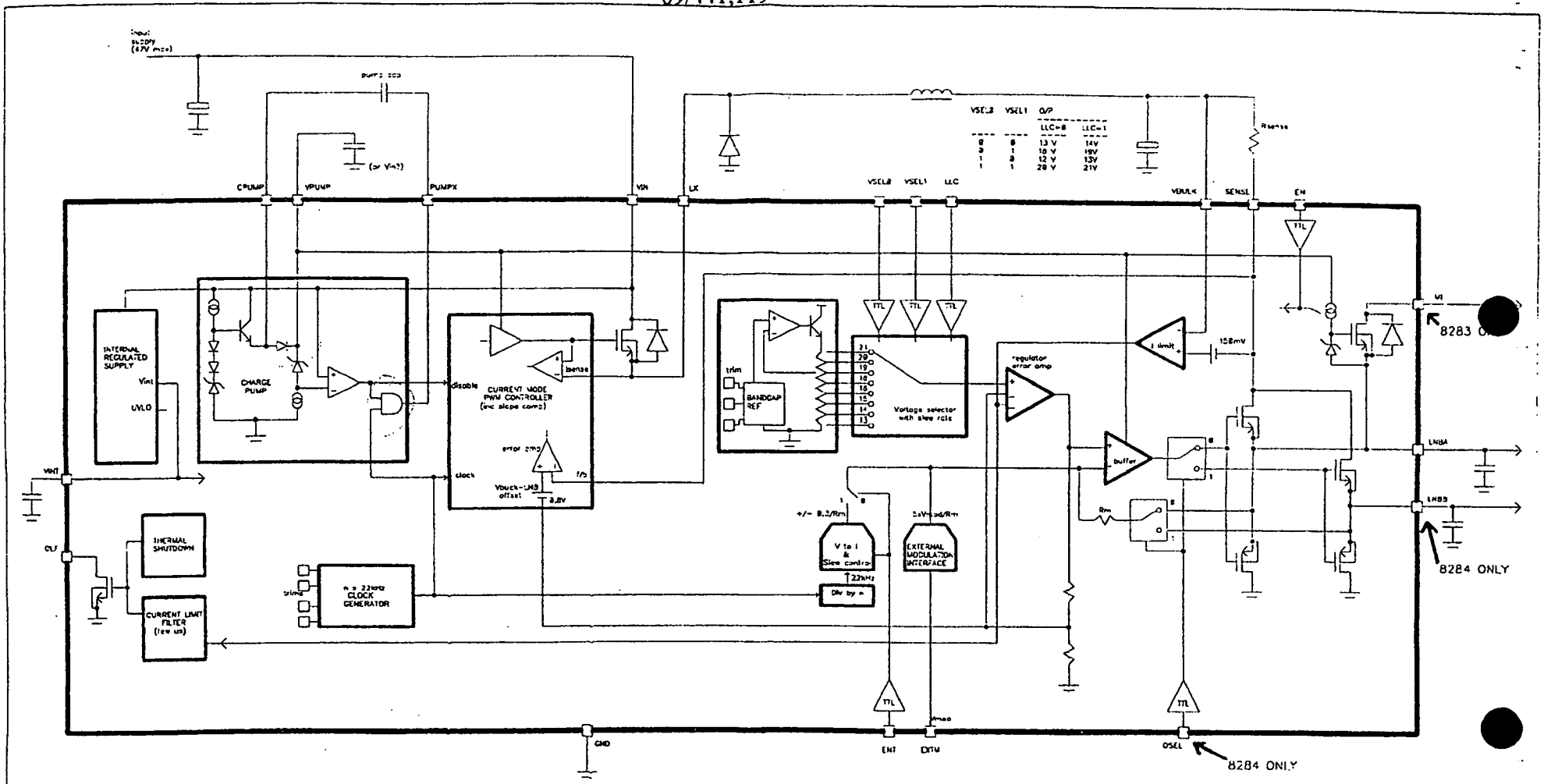


Exhibit B to 1.131 Declaration
U.S. Patent Application No.
09/441,119



LNB BUCK REGULATOR PROPOSAL – 31st March 1999

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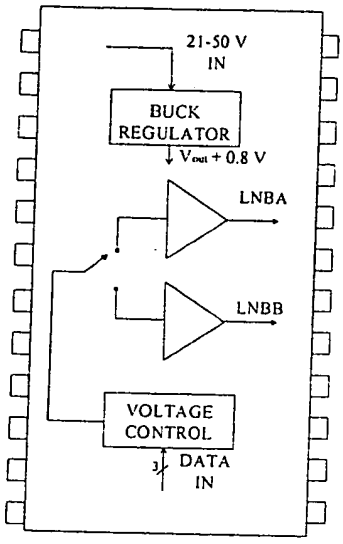
Interim Data Sheet



Two Output LNB Supply and Control Voltage Regulator

- Complete interface for two LNBs remote supply and control
- LNB selection and stand-by function
- Built-in tone oscillator factory trimmed to 22 kHz facilitates DiSEqC™ encoding
- Full modulation with no load
- Tracking switch-mode power converter for lowest dissipation
- Externally adjustable short-circuit protection
- LNB short-circuit protection and diagnostics
- Auxiliary modulation input
- Cable length compensation
- Internal over temperature protection
- Reverse current protection

Intended for analog and digital satellite receivers, the low noise block converter regulator (LNBR) is a monolithic linear and switching voltage regulator, specifically designed to provide the power and the interface signals to the LNB downconverter via the coaxial cable. Because most satellite receivers have two antenna ports, the output voltage of the regulator is available at one of two logic-selectable output terminals (LNBA, LNBB). If the device is in stand-by mode (EN terminal LOW), both regulator outputs are disabled. This is to allow the antenna downconverters to be supplied and controlled by other satellite receivers sharing the same coaxial cable. In this mode the device will limit reverse current to 3 mA.

The regulator outputs are set to 12, 13, 18, or 20 volts by the VSEL terminals. Additionally, it is possible to increase by 1 V the selected voltage to compensate the voltage drop in the coaxial cable (LLC terminal HIGH).

Cont....

ABSOLUTE MAXIMUM RATINGS

DC Input voltage	50 V
Output Current	Internally limited
Logic Input Voltage	-0.5 to 7 V
Storage temperature range	-40 to 150°C
Operating Junction Temperature Range	-40 to 150°C

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The LNBR is a combination of a tracking switching regulator and low-noise linear regulators. Logic inputs (VSEL0, VSEL1 and LLC) select the desired output voltage. A tracking current-mode buck converter provides the linear regulator input voltage that is set to the output voltage plus typically 0.8 volt. This maintains constant voltage drop across the linear regulators while permitting adequate voltage range for tone injection.

The ENT (Tone Enable) terminal activates the internal tone signal modulating the dc output with a $\pm$ 0.3 V, 22 kHz symmetrical waveform. The internal oscillator is factory trimmed to provide a tone of 22 kHz $\pm$ 2 kHz. No further adjustment is required. The internal oscillator operates the buck converter at 16 times the tone frequency.

Burst coding of the 22 kHz tone can be accomplished, due to the fast response of the ENT input and rapid tone response. This allows implementation of the DiSEqC™ protocols.

To improve design flexibility and to allow implementation of proposed LNB remote control standards, an analog modulation input terminal is available (EXTM). An appropriate dc blocking capacitor must be used to couple the modulating signal source to the EXTM terminal. If external modulation is not used, the EXTM terminal can be left open.

The output linear regulators will sink and source current. This feature allows full modulation capability into capacitive loads as high as 250 nF.

The programmed output voltage rise and fall times can be set by an internal 50 k Ω resister and an external capacitor located on the TCAP terminal. Although any value of capacitor is permitted, practical values are typically 1 nF to 20 nF. This feature only affects the turn on and programmed voltage rise and fall times. Modulation is unaffected by the choice of TCAP. This terminal can be left open if voltage rise and fall time control is not required.

Two terminals are dedicated to the over current protection/monitoring: SENSE and OLF. The LNB output is current limited. The short-circuit protection threshold is set by the value of an external resistor, Rsense. Rsense = 0.15/Imax where Imax is the desired current limit. The minimum safe value for Rsense is 0.22 ohm

In operation the short-circuit protection produces current fold-back at the input due to the tracking converter. If the output is shorted the linear regulator will limit the output current to Imax. The tracking converter will maintain a constant voltage drop of 0.8 volts across the linear regulator. This condition results in (Imax)*(0.8 volts) or typically 550 mW dissipation. Short-circuit or thermal shutdown activation will cause the OLF terminal, an open-drain diagnostic output flag, to go LOW.

The device is packaged in a 24 DIP or an SOIC power-tab package.
Thermal resistance: DIP $R_{\theta JA}$=40°C/W, $R_{\theta JT}$=6°C/W,SOIC $R_{\theta JA}$=55°C/W, $R_{\theta JT}$=6°C/W

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DiSEqC™ is a trademark of EUTELSAT.

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Terminal Configuration

Symbol	Terminal	Function
VINT		Bypass capacitor for internal voltage reference
CPUMP		High side of charge-pump cap
EN		Logic input: enables switcher and outputs
ENT		Logic input: enable internal modulation
EXTM		External modulation input
GND		Ground
VBULK		Tracking supply voltage to linear regulators
LLC		Logic input: increases output voltage by 1 V for line length
Voa		LNBA output voltage A
Vob		LNBB output voltage B
LX		Inductor drive point
SENSE		Current limit setup resistor
OLF		Overload flag output
OSEL		Logic input: selects between LNB, A or B
VIN or Vcc		Supply input voltage (range VLNB+2.5 V to 47 V)
VPUMP		Gate supply voltage for high side drivers
PUMPX		Charge-pump drive
TCAP		Capacitor for setting the rise and fall time of the outputs
VSEL0		Logic input: output voltage select
VSEL1		Logic input: output voltage select

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Electrical Characteristics for LNBR Series (T_A = 25°C, ENT=L, EN=H, LLC=L, V_{IN}=24 V, Iout=50 mA (unless otherwise specified).

Symbol	Parameter	Test Conditions	Min.	Typ.	Max	Unit
V_{IN}	V_{cc1} Supply Voltage	I_O=600 mA,VSEL0=L,VSEL1=L, LLC=L	2.5+V_o		47	V
V_{O1}	Output Voltage	I_O =600 mA,VSEL0=L,VSEL1=H, LLC=L Io=600 mA, SEL0=L,VSEL1=H, LLC=H	17.3	18 19	18.7	V V
V_{O2}	Output Voltage	I_O=600 mA, VSEL0=L,VSEL1=L LLC=L I_O=600 mA, VSEL0=L,VSEL1=L, LLC=H	12.5	13 14	13.5	V V
V_{O1}	Output Voltage	I_O=600 mA,VSEL0=H,VSEL1=H, LLC=L Io=600 mA, SEL0=H,VSEL1=H, LLC=H		20 21		V V
V_{O2}	Output Voltage	I_O=600 mA, VSEL0=H,VSEL1=L LLC=L I_O=600 mA, VSEL0=H,VSEL1=L, LLC=H		12 13		V V
ΔVO	Line Regulation	V_o=13 V, V_{IN}=16 to 40 V V_o=18 V ,V_{IN}=21 to 40 V		4.0 4.0	40 40	mV mV
ΔVO	Load Regulation	V_o=13 or 18 V I_o=50 to 600 mA		80	180	mV
SVR	Supply Voltage Rejection	f_{AC}=100 Hz		45		dB
I_{MAX}	Output Current Limiting	Rsense=0.22 ohm	630	680	730	mA
f_{TONE}	Tone Frequency	ENT=H	20	22	24	kHz
a_{TONE}	Tone Amplitude	ENT=H	0.55	0.68	0.8	Vpp
d_{TONE}	Tone duty cycle	ENT=H	40	50	60	%
t_R, t_F	Tone rise or fall time	ENT=H	5.0	10	15	µs
g_{EXTM}	External modulation gain	$\Delta V_O/\Delta V_{EXTM}$, f=10 Hz to 40 kHz		1.0		V/V
V_{EXTM}	External modulation input voltage	AC coupling			0.8	Vpp
Z_{EXTM}	External modulation input impedance	f=10 Hz to 40 kHz		5		k Ω
V_{OL}	Overload flag terminal logic low	I_{OL}=8.0 mA		0.28		V
I_{OZ}	Overload flag terminal OFF state leakage current	V_{OH}=6.0 V		< 1.0		µa
V_{IL}	Control input terminal logic low				0.8	V
V_{IH}	Control input terminal logic high		2.0			V
I_{IH}	Control terminals input current	V_{IH}=5 V		< 1.0		µA
I_{CC}	Supply current	Outputs disabled (EN=L)		.5		mA
I_{CC}	Supply current	ENT=H, I_{OUT}=600 mA V_o=13		382		mA
I_{OBK}	Output reverse current	EN=L, V_{LNBA}=V_{LNBB}=18 V V_{IN1}=V_{IN2}=22 V or floating		1.0		mA
T_{SHDN}	Thermal shutdown threshold			165		°C
ΔV_{BUCK}	Linear regulator voltage drop	V_{BULK} -V_o		0.8		V
f_o	Switching frequency	f_{TONE} * 16	320	352	384	kHz

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Truth Tables

Control I/O	Terminal Name	L	H
OUT	OLF	Iout > Iomax or Tj > 165°C	Iout < Iomax and Tj < 130°C
IN	ENT	22 kHz tone OFF	22 kHz tone ON

SEL	VSEL0	VSEL1	LLC	V_{LNBA} (typ.)	V_{LNBB} (typ.)
L	L	L	L	13 V	Low
L	L	H	L	18 V	Low
L	L	L	H	14 V	Low
L	L	H	H	19 V	Low
H	L	L	L	Low	13 V
H	L	H	L	Low	18 V
H	L	L	H	Low	14 V
H	L	H	H	Low	19 V
L	H	L	L	12 V	Low
L	H	H	L	20 V	Low
L	H	L	H	13 V	Low
L	H	H	H	21 V	Low
H	H	L	L	Low	12 V
H	H	H	L	Low	20 V
H	H	L	H	Low	13 V
H	H	H	H	Low	21 V

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